FW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,220	11/28/2000	Farhad Fouladi	723-974	7835

27562 7590 06/02/2005

NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,220	FOULADI ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,16-23,25,27-37,39,40 and 43-53* is/are rejected.

7)☒ Claim(s) *13,15,24,26,38,41 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-04-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated February 4, 2005 in response to PTO Office Action dated August 4, 2004. The amendments to claim(s) 1, 5-8, 10, 12, 13, 16-19, 21-24, 27, 30-33, 36, 39, 40, 43, 46-49, 52 and 53 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

2. Applicant's arguments filed February 4, 2005 with respect to the rejection(s)of claim(s) 1-12, 14, 16-23, 25, 27-35, 37, 39, 40, 43-51 and 53 under 35 U.S.C. 103(a) have been fully considered and are persuasive as the U.S. Patent No. 6,564,304 to Harriman et al. has a filing date of September 1, 2000 while applicant claims priority to a provisional application filed on August 23, 2000, which is prior to the filing date of Harriman et al. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S. Patent No. 6,092,158 to Harriman et al.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-7, 16-18, 27-30, 39, 43-46 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,295,586 B1 to Novak et al. in view of U.S. Patent No. 6,092,158 to Harriman et al.

a. Regarding claim 1, Novak et al. **discloses** a queue based memory controller (MCT 200) comprising: a plurality of buffer memories (PQ 350, read/write operation

queue (RWQ) 360, Fig. 2), each of said buffer memories being operatively coupled to one of said plurality of resources (memory requestors 210, Fig. 1) seeking access to said memory for storing information indicative of a request for memory access (...the northbridge 60 is designed to interconnect the memory 70...typically these devices include the CPU...I/O devices...these devices are also known as memory requesters 210...which then executes and completes these requests to the memory...col. 5, lines 1-40); a multiple resource buffer memory (RWCQ 365) coupled to said first plurality of buffer memories (PQ 350, RWQ 360) for storing requests for memory access requests from each of said plurality of resources (memory requestors 210) (...the operation queues are 340, 350, 360 are interconnected with each other and the RWCQ 365 in order to track and properly issue operations currently in the operation queues 340, 350, 360...once the memory request is initiated, the RWCQ 365 is responsible for tracking the outstanding read or write operations that have been sent to the memory 70...col. 5, lines 1-40). Although, RWCQ 365 includes control logic 460, which is used for tracking read or write operations a control circuit for controlling the transfer of information from said first plurality of buffer memories (PQ 350, RWQ 360, Fig. 2) to said multiple resource buffer memory (RWCQ 365, Fig. 2), it **does not disclose** the means to reduce the frequency of switching from main memory write operations to main memory read operations. Harriman et al. **discloses** separation of read and write accesses to optimize overall memory access times by grouping reads and writes to reduce bus turn around (...grouping reads and writes may also reduce "turn around"...col. 1, lines 35-50) similar to instant claim limitation "to reduce the frequency of switching from main memory write operations to main memory read operations". Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Novak et al. with the feature "reducing frequency of switching

from main memory write operations to main memory read operations i.e., mode or context switching by grouping reads and writes" as taught by Harriman et al. **because** it results in an improved and optimized overall memory access performance.

b. Regarding claim 2, Novak et al. **discloses** wherein said plurality of buffer memories are main memory write queues (PQ 350, RWQ 360, Fig. 2).

c. Regarding claim 3, Novak et al. **discloses** wherein said multiple resource buffer memory is a main memory write queue (RWCQ 365, Fig. 2).

d. Regarding claim 4, Novak et al. **discloses** wherein said control circuit (control logic 460, Fig. 2) is operable to control the rate at which write requests are coupled to the multiple resource buffer memory (RWCQ 365, Fig. 2) from the plurality of buffer memories (PQ 350, RWQ 360, Fig. 2)(...on each cycle, as the VRd 450 and the VWr 455 shift down, the appropriate control signals for the current cycle enter the bottom queue entry...and are dispatched to control the appropriate actions in the SMC 230...col. 9, lines 50-61).

e. Regarding claim 5, Novak et al. **discloses** further including a plurality of main memory read queues (PQ 350, RWQ 360, Fig. 2).

f. Regarding claim 6, Novak et al. **discloses** arbitration circuitry (memory request arbiter MRA 220, Fig. 1) for granting requests for access to main memory (memory 70, Fig. 2).

g. Regarding claims 7, 18, 30 and 46, Novak et al. **discloses** wherein said arbitration circuitry (memory request arbiter MRA 220, Fig. 1) is operable to control the frequency with which the requesting resources are enabled to participate in the arbitration for main memory access (...the memory requesters 210 make various

requests on the inputs of the MRA 220 for access to the memory 70. The MRA 220 selects one request to be sent to the SMC 230...col. 8, lines 20-22).

h. Regarding claim 16, it is similar in scope to claim 1 above and is rejected under the same rationale.

i. Regarding claim 17, it is similar in scope to claim 1 above and is rejected under the same rationale.

j. Regarding claims 27 and 43, the claim limitation stating delaying forwarding requests for memory access to reduce the frequency of switching between memory read states and memory write states; and granting requests for memory access is similar in scope to claim 1 and is rejected under the same rationale.

k. Regarding claims 28 and 44, Novak **discloses** storing requests in a multiple resource write queue (RWCQ 365, Fig. 2).

l. Regarding claims 39 and 53, Novak **discloses** fulfilling requests for memory access in the order requested (...the operation queues...issue their queued...memory operations...the operation queues monitor and adhere to timing and ordering dependencies...that are queued...Abstract)

m. Regarding claim 29, it is similar in scope to claim 28 and is rejected under the same rationale.

n. Regarding claim 44, it is similar in scope to claim 28 above and is rejected under the same rationale.

o. Regarding claim 45, it is similar in scope to claim 29 above and is rejected under the same rationale.

2. Claims 8-12, 19-23, 31-35 and47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,295,586 B1 to Novak et al. in view of U.S. Patent No.

6,092,158 to Harriman et al. as applied to claim 1 above and further in view of U.S. Patent No. 6,330,647 B1 to Jeddeloh et al.

a. Regarding claims 8, 19, 31 and 47, Novak-Van Hook combination **fails to disclose** including a memory access control register associated with one of said resources, wherein said arbitration control circuit includes arbitration circuitry responsive to the contents of said memory access control register for determining the frequency that said resource is permitted to participate in memory access arbitration. Jeddeloh et al. **discloses** an arbiter 210 in combination with configuration registers 214 to record access count values for each requestor (resources or class of requester) and counters 214 may be used by arbiter 210 to track the number of memory access operations remaining for a selected requester (col. 3, lines 53-67; col. 4, lines 1-30). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made modify the Novak-Van Hook combination with the feature "memory configuration register that determines the frequency that a said resource is permitted to participate in memory access arbitration" as taught by Jeddeloh et al. **because** it provides for efficient memory access control without denying access to those requestors issuing single access transactions and/or low priority requests for an unacceptable long time (col. 1, lines 48-51).

b. Regarding claims 9, 20, 32 and 48, Novak-Van Hook as modified by Jeddeloh et al. **discloses** said control registers (configuration registers 212) being programmable by said main processor (system controller 102)(...system controller 102 ..may...set and adjust requestor access count values...(i.e., modify values stored in configuration register 212...col. 5, lines 1-10).

c. Regarding claims 10, 21, 33 and 49, Novak-Van Hook as modified by Jeddeloh et al. **discloses implicitly**, wherein said control registers include a plurality of memory

bandwidth control registers which are accessed by said control circuitry in determining which resource will be granted memory access (...count values may be determined dynamically at...system start up and/or modified during system operations...access count values may be based on requestor operating speed, wherein faster devices are allocated larger access count values...col. 5, lines 1-10).

d. Regarding claims 11, 22, 34 and 50, Novak-Van Hook as modified by Jeddeloh et al. **discloses** wherein each of said memory bandwidth control registers (configuration registers 212) is respectively associated with a resource seeking main memory access (...configuration registers 212 may be used to record access count values for each requestor (or class of requestor)...col. 4, lines 1-6.

e. Regarding claims 12, 23, 35 and 51, Novak-Van Hook as modified by Jeddeloh et al. **discloses implicitly** at least one register for said requesting resource indicative of at least one of memory usage and memory bandwidth for that resource (...configuration registers 212 may be used to record access count values...counters 214 may be used by arbiter 210 to track number of memory access operations...col. 4, lines 1-6).

3. Claims 14, 25, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,295,586 B1 to Novak et al. in view of U.S. Patent No. 6,092,158 to Harriman et al. as applied to claim 1 above and further in view of U.S. Patent No. 5,666,494 B1 to Mote, Jr.

a. Regarding claims 14, 25 and 37, Novak-Van Hook **is silent about** a resource that is writing to main memory generating a flush signal for initiating the flushing of that resource's write request queue. Mote, Jr. **discloses** a memory subsystem utilizing a queue mechanism and flushing of posted write buffer to write the write data to the memory (DRAMs 135). The instant application specification at page 32, lines 18-21 discloses flushing of the write buffer WQ0 to main memory 112 resulting in writing to the identified address location similarly as per the instant claim limitation. Therefore, it

would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Novak-Van Hook combination with the feature "flushing of the write buffer" as taught by Mote, Jr. **because** it results in most current data to be retrieved from the memory instead of state data.

b. Regarding claim 40, it is similar in scope to claim 14 above and is rejected under the same rationale.

Allowable Subject Matter

4. Claims 13, 24, 36 and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art fails to particularly disclose a register indicative of wasted memory cycles due to granting memory access to that resource.

5. Claims 15, 26, 38, 41 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(571) 272-7778**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dalip K. Singh
Examiner , Art Unit 2676

dks
May 30, 2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600